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PTO-1449 (Modified) U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO.	SERIAL NUMBER
	211.001-D4-US	10/727,742
	APPLICANT(S)  Fazan et al.	
FILING DATE  December 4, 2003	GROUP ART UNIT	

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JM	5,448,513	9/1995	Hu et al.	365	150	
JM	4,298,962	11/1981	Hamano et al.	365	182	
JM	3,439,214	4/1969	Kabell	315	11	
JM	6,081,443	6/2000	Morishita	365	149	
JM	6,111,778	8/2000	MacDonald et al.	365	149	

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JM	FR 2 197 494	3/1974	French			
JM	EP 1 180 799	2/2002	European			
JM	EP 0 030 856	6/1981	European			
JM	GB 1 414 228	11/1975	Great Britain			
JM	EP 0 694 977	1/1996	European			
JM	JP 02 294076	2/1991	Japanese			
JM	EP 1 237 193	9/2002	European			
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
<i>JM</i>	EP 0 801 427	10/1997	European			
<i>JM</i>	EP 0 513 923	11/1992	European			

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<i>JM</i>	EP 0 731 972	11/2001	European			
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<i>JM</i>	"Mechanisms of Charge Modulation in the Floating Body of Triple-Well nMOSFET Capacitor-less DRAMs", Villaret et al., Proceedings of the INFOS 2003, Insulating Films on Semiconductors, 13th Bi-annual Conference, June 18-20, 2003, Barcelona (Spain), (4 pages)

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JHC	2002/0076880	6/2002	Yamada et al.			
JHC	2002/0098643	7/2002	Kawanaka et al.			
JY	2002/0110018	8/2002	Ohsawa			
JY	2002/0114191	8/2002	Iwata et al.			
JY	2002/0130341	9/2002	Horiguchi et al.			
JY	2002/0160581	10/2002	Watanabe et al.			
JHC	2003/0003608	1/2003	Arikado et al.			
JHC	2003/0015757	1/2003	Ohsawa			
JHC	2003/0035324	2/2003	Fujita et al.			
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<i>JM</i>	"One of Application of SOI Memory Cell – Memory Array", Lončar et al., IEEE Proc. 22 <sup>nd</sup> International Conference on Microelectronics (MIEL 2000), Vol. 2, NIŠ, Serbia, 14-17 May 2000, pp.455-458
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<i>JM</i>	"Chip Level Reliability on SOI Embedded Memory", Kim et al., Proceedings 1998 IEEE International SOI Conference, Oct. 1998, pp.135-139

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<i>JM</i>	"Measurement of Transient Effects in SOI DRAM/SRAM Access Transistors", A. Wei, IEEE Electron Device Letters, Vol. 17, No. 5, May 1996, pp.193-195
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<i>JKW</i>	"A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation", Assaderaghi et al., IEEE IEDM, 1994, pp.809-812
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<i>JM</i>	"3-Dimensional Simulation of Turn-off Current in Partially Depleted SOI MOSFETs", Ikeda et al., IEIC Technical Report, Institute of Electronics, Information and Communication Engineers, 1998, Vol. 97, No. 557 (SDM97 186-198), pp.27-34

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	APPLICANT(S) Fazan et al.	
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	<b>211.001-D4-US</b>	<b>10727,742</b>
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JKL	2002-343886	11/2002	Japanese			X
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